REMARKS

This amendment is submitted in response to the Examiner's Action dated March 19, 2004. Applicants have provided a new title and have amended the claims to clarify key features of the invention and overcome the claim rejections. No new matter has been added, and the amendments place the claims in better condition for allowance. Applicants respectfully request entry of the amendments to the claims. The discussion/arguments provided below reference the claims in their amended form.

IN THE TITLE

In the present Office Action, Examiner states that the title of the invention is not descriptive. Accordingly, Applicants have rewritten the title to be more clearly descriptive of the invention to which the claims are directed. Applicants respectfully request entry of the new title and withdrawal of the objections thereto. Applicants have also corrected grammatical and typographical errors, etc., within the specification.

ALLOWABLE SUBJECT MATTER

At paragraph 27 of the present Office Action, Examiner states that Claims 12-13, 18-21 and 26-28 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Applicants have amended the independent claims to more completely described the novel features of the invention and overcome the rejections of those claims. Since the amendments and supporting arguments overcome the rejections of the independent claims, all claims are now in condition for allowance. Applicants, therefore, respectfully request Examiner extend the allowance to include all pending claims.

CLAIMS REJECTIONS UNDER 35 U.S.C. § 112

At paragraph 7 of the Office Action, Claim 11 is rejected under 35 U.S.C. § 112, second paragraph. Claim 11 has been amended to correctly depend on Claim 10, thus making all features of Claim 11 definite. The amendment overcomes the §112 rejection, and Applicants respectfully request reconsideration of the rejection in light of the amendment.

DOUBLE PATENTING

At paragraph 6 of the present Office Action, Claims 1-2 and 8-9 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 5 of U.S. Patent No, 6,606,702.

At paragraph 7 of the present Office Action, Claims 10 and 22 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 6 of U.S. Patent No, 6,606,702.

At paragraph 9 of the present Office Action, Claims 3-5, 11, 15 and 23 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 7 of U.S. Patent No, 6,606,702.

Applicants submit herewith a terminal disclaimer in compliance with 37 CFR 1.321(c). This filing overcomes the double patenting rejection. Applicants, therefore, respectfully request removal of the double patenting rejection to the above claims.

CLAIMS REJECTIONS UNDER 35 U.S.C. § 102

In the present Office Action, Claims 1-3 and 8-9 are rejected under 35 U.S.C. § 102(e) as being anticipated by *Morris, et al.* (U.S. Patent No. 6,286,095). *Morris* does not anticipate Applicants' claimed invention because *Morris* does not teach each feature recited by Applicants' claims.

Applicants' invention is directed to a processor operation that enables instructions (e.g., read instructions) that are sequentially after a barrier operation within an instruction stream to be issued for execution prior to the completion of the barrier operation. Results generated by the instructions are tagged along with the instructions/processes as being speculative and a (multiprocessor speculation) flag is set within corresponding register(s) to signal the speculative nature of the instructions execution and resulting data/results. Notably, as utilized by Applicant's invention, the term "speculative" or "barrier-speculative" refers solely to the fact that the instructions are issued before the preceding barrier instruction has been completed. That term is differentiated within the specification and claims from execution within a branch path that is speculatively taken during branch prediction.

Applicants' claims recite the following features:

(1) "speculatively executing operations associated with instructions sequentially following said barrier operation in an instruction sequence prior to completion of said barrier operation, wherein **operations are speculatively executed relative to a preceding barrier operation** whenever the preceding barrier operation has **not yet completed;**" and

(2) "**immediately forwarding data** returned by a load instruction among said instructions sequentially following said barrier operation **to execution units** of said processor, wherein said data is utilized within said operations, where necessary, **regardless of a completion status of said barrier operation**, wherein further, said operations and results/data generated by said operations are **tagged as barrier-speculative** when said operations are speculatively executed **relative to the barrier operation,**" (emphases added).

Morris, in contrast, provides a special instruction to force ordered load and store operations. *Morris* teaches the exact opposite of the functionality provided by Applicants' invention. As stated in the Abstract, *Morris* provides "incorporating special instructions to force load and store operations to execute in program order." Further, "[a] new load instruction is provided which blocks any subsequent load instructions from executing until this load instruction has been completed by an associated CPU."

The cited sections of *Morris* (col. 4, lines 10-37) provide a description of "a new load instruction ... that prevents the CPU from performing subsequent load operations until its load operation is completed" and "the new instructions provide the needed synchronization, while ... allowing the CPU to execute subsequent unrelated operations." Column 6, lines 21-23 states that "since there is a prior store instruction pending, the ordered store is suspended until after the pending mailbox store is completed."

Clearly, these sections teach away from "immediately forwarding data returned by a load instruction to execution units of said processor, ... regardless of a completion status of said barrier operation, ... tagged as barrier-speculative when said operations are speculatively executed relative to the barrier operation."

Morris does not teach executing processes, including load instructions, beyond preceding barrier operations that have not yet completed. Examiner references a sentence in *Morris* which states that the instructions allow "executing subsequent instructions while waiting for a prior instruction to complete." However, there is no mention or reference of executing instructions beyond a branch instruction. At the time of Applicants' invention, executing instructions out of order and/or concurrent/overlapping execution of instructions was known in the art. What was not know in the art and is not taught by *Morris* is execution beyond barrier operations, and particularly execution of a load request and operations with the data returned by the load request beyond a preceding barrier operation.

The standard for a § 102 rejection requires that the reference teach each element recited in the claims set forth within the invention. As clearly outlined above, *Morris* fails to meet this standard and therefore does not anticipate Applicants' invention.

CLAIM REJECTIONS UNDER 35 U.S.C. § 103

In the present Office Action, Claims 4-5 and 10-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Morris* in view of *Hesson, et al.* (U.S. Patent No. 5,615,350). Claims 6-7, 14-17 and 22-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Morris* in view of *Hesson, et al.* and in further view of *Tran* (U.S. Patent No. 5,822,575).

Claim 22 is an independent claim and includes some of the allowable features of Claim 1. The other claims are all dependent on independent claims, which Applicants have shown are allowable over *Morris*. The allowability of the independent claims from which the present claims depend renders the present claims allowable.

The deficiencies of *Morris* have been described above. Applicants also note the following deficiencies with regards to the other references and combinations thereof.

Hesson provides an out of order execution of load-store instructions. The cited section of *Hesson* (namely col. 3, lines 64- col. 4, lines 16) provides a description of a store barrier cache that permits "speculative execution of load and store instructions." The cache contains "history

bits that are used to predict the condition wherein a load instruction has executed ahead of a store instruction in program order and that the data structure of the load and store instruction have a same real address" (*emphasis added*; ll 4-9). If a store-load conflict is predicted, a barrier bit is marked during dispatch of the store instruction "so that no loads in program order are permitted to execute ahead of the store that is predicted to be violated." (ll 9-15). Process block 59 of Figure 2B states: "reset the store barrier control bit in the rename unit so that load instructions that follow the store that were held up by the store barrier bit can once again issue." Examiner admits that *Hesson* does not have specific barrier operations. Clearly, the use of a bit to illustrate the load operation is issued out of order with respect to a load operation does not convey or suggest a bit that enables data/results and processes to be tagged as barrier-speculative.

One skilled in the art would not find the above description (of issuing loads out of order with respect to stores and tagging to indicate such out of order issuance) to be suggestive of issuing loads speculatively with respect to a preceding barrier operation. One could conceivably include the features of *Hesson*'s invention in a processor implementing Applicants' invention as totally independent features with little or no overlap in functionality.

Tran provides a discussion of traditional speculative branch prediction and never mentions or suggests speculation beyond a preceding barrier operation. Notably, Examiner states that when branch instructions are mis-predicted, the instructions executed after the branch instruction must be discarded. Applicants claimed invention, however, actually re-executes the instructions and discards only the results of those instructions that relied on data that may have been affected by the barrier operation (see Claim 5). Since *Tran* does not contemplate or suggest speculative issuance with respect to a preceding barrier operation, *Tran* does not suggest the features of Claim 7 related to embedded speculative load issuance with a branch.

Given the above reasons, it is clear that the combinations of the above references would not suggest key features of Applicants' claims. One skilled in the art would not find Applicants' claimed invention unpatentable over the combination of references. The above claims are therefore allowable over the combination.

CONCLUSION

Applicants have diligently responded to the Office Action by amending the claims to clarify features recited by the claims and overcome the respective claim rejections. Applicants have further submitted herewith a terminal disclaimer to overcome obviousness-type double patenting rejection. The amendments and arguments supporting allowability of the claims overcome the §112, §102 and §103 rejections, and Applicants, therefore, respectfully request issuance of a Notice of Allowance for all claims now pending.

Applicants further requests the Examiner contact the undersigned attorney of record at 512.343.6116 if such would further or expedite the prosecution of the present Application.

Respectfully submitted,

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